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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,986	09/12/2003	Louis K. Scheffer	CA7016672001	6083

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,986	SCHEFFER, LOUIS K.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/03;7/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/660,986 filed on 9/12/2003. Claims 1-33 remain pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-14, 16-25 and 27-33 are rejected under 35 U.S.C. 103(a) as being obvious over Smits et al. (6,631,444).

4. As to claims 1, 12 and 23, Smits et al. teach an IC design that provides a solution to a synchronization and timing problems inherent in the IC design of a very large, on-die memory operating with a high-speed processor core in pipelined fashion (see field of the invention, col. 2, lines 39-58, and Fig. 2, 4-5 and its detailed description). The problems arise when some of the banks are located relatively close to central location and other banks are located relatively far from central location (col. 5, lines 60-67, col. 3, lines 20-33). In order to resolve synchronization and timing problems along bus lines operating in pipelined fashion, Smits et al. teach inserting number of flip-flips, buffers or latches along the bus lines (rules for pipelining) or at specified one or more pipeline locations of the IC design (electronic design) (Fig. 4-5, col. 5 line 60 to col. 7 line 30). Thus, Smits et al. teach generating an electronic design (IC design); specifying one or more pipeline locations and modifying the one or more pipeline locations. Smits et al. do not teach communicating a result of modifying to a user. In order accurately verify the IC design in

compliance with design constraints (synchronization and timing constraints) as expected, it would have been obvious to one ordinary skill in the art at the time the invention was made to have included communicating a result of modification to a user (designer).

5. As to claims 2-3, 13-14 and 24-25, Smits et al. teach specifying rules for pipelining (col. 6, lines 1-9, number of inserted flip-flops, buffers or latches); organizing signals in one or more pipeline locations into signal groups (Fig. 4-5).

6. As to claims 5-8, 11, 16-19, 22, 27-30 and 33, Smits et al. inserting number of clocked elements in the one or more pipeline locations of IC design in order to provide synchronization and in compliance with timing constraints using placement tool (well known floorplan or layout tool or placeholders in IC design), where the number of inserted clocked elements are based on distances (parameter, length parameters) between banks and processor core (Fig. 4, col. 5 line 30 to col. 7 line 30).

7. As to claims 9, 20 and 31, Smits et al. resolving synchronization and timing problems in IC design operating in pipelined fashion by inserting number of clocked elements in the one or more pipeline locations of IC design in order to provide synchronization and in compliance with timing constraints using placement tool (well known floorplan or layout tool or placeholders in IC design), where the number of inserted clocked elements are based on distances (parameter, length parameters) between banks and processor core (Fig. 4, col. 5 line 30 to col. 7 line 30). As shown in Fig. 4 and described in the patent, number of inserted clocked elements depends on relative distances between banks and the processor core. Such number of inserted clocked elements based distances between the banks and processor core are determined in order to provide an IC design that comply with synchronization and timing constraint. These teachings

correspond to converting timing parameters into length parameters. it depend how relatively distance of the banks where the locations of the banks are

8. As to claims 10, 21 and 32, in order to design an IC that includes inserting of clocked elements based distances between banks and processor core (act of modification of IC design) in order to provide synchronization and in compliance with timing constraints, a master design must be modified to include such modified design (inserted clocked elements) in order to obtain a final master design for final verification and lastly for IC design fabrication.

9. Claims 4, 15 and 26 are rejected under 35 U.S.C. 103(a) as being obvious over Smits et al. (6,631,444) in view of DiGiacomo et al. (4,630,219).

10. As to claims 4, 15 and 26, Smits et al. teach specifying a minimum number and a maximum number of clocked elements for the one or more pipeline locations, specifying a clocked element and a clock (Fig. 4, number of inserted flip flops or latches) except insertion cost. The insertion cost is taught by DiGiacomo et al. (Fig. 47 and its description; col. 33, lines 23-29; col. 34, line 31-57). The insertion cost is calculated before inserting an unplaced component during placement operation. The component with lowest cost value is picked as a candidate for placement when other design requirements have been met. Therefore, combining these above teachings would have obvious to one of ordinary skill in the art at the time the invention was made because insertion cost must be evaluated before placing any component (inserting of clocked elements) that is in compliance with design rule requirements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER